VERIFICATION OF TRANSLATION

I, Kil-Sung SON, of Suite 1810, Hwanghwa Bldg., 832-7, Yeoksam-dong, Gangnam-gu, Seoul, Republic of Korea hereby declare that I am knowledgeable in the English and Korean languages, and that to the best of my knowledge the attached document is true and complete English translation of the patent application of Korean Patent Application No. 2002-50246.

Dated 28th of April, 2005

Kil-sung Son

Signature

SPECIFICATION

[Title of the Invention]

Bitline of semiconductor device having stud type capping layer and method for fabricating the same

[Brief Description of the Drawings]

Fig. 1 is a layout of a semiconductor device having a prior COB structure.

Fig. 2a through Fig. 2d are process sectional views illustrating a fabricating method of a prior semiconductor device in accordance with a 1A-1A' line of Fig. 1.

Fig. 3a through Fig. 3d are process sectional views illustrating a fabricating method of a prior semiconductor device in accordance with a 1B-1B' line of Fig. 1.

Fig. 4 is a sectional structure chart of a prior semiconductor device in accordance with a 1C-1C' line of Fig. 1.

Fig. 5a through 5i are process sectional views illustrating a fabricating method of a semiconductor device in accordance with one embodiment of the

present invention.

Fig. 6a through 6i are process sectional views illustrating a fabricating method of a semiconductor device in accordance with one embodiment of the present invention.

Fig. 7a through Fig. 7i are process sectional views illustrating a fabricating method of a semiconductor device in accordance with one embodiment of the present invention.

Fig. 8a through Fig. 8d are process sectional views illustrating a fabricating method of a semiconductor device in accordance with another embodiment of the present invention.

Fig. 9a through 9d are process sectional views illustrating a fabricating method of a semiconductor device in accordance with another embodiment of the present invention.

Fig. 10a through 10d are process sectional views illustrating a fabricating method of a semiconductor device in accordance with another embodiment of the present invention.

Fig. 11a is a diagram showing relations between thickness of a bitline capping layer and parasitic capacitance.

Fig. 11b is a diagram showing relations between a bitline spacer and parasitic capacitance.

[Detailed Description of the invention]

[Object of the Invention]

[Technical field of the invention and Related Art prior to the Invention]

The present invention generally relates to a bitline structure of a semiconductor device, and more specifically, to a damascene bitline structure of a semiconductor device and a method for fabricating the same for reducing parasitic capacitance by forming a capping layer in a stud type and for improving process margins.

As the size of a semiconductor device has been reduced, line width of a bitline, a data line has also been decreased, thereby increasing bitline resistance. To solve a problem of the increased resistance of the bitline, a metal film like tungsten is used with the use of bitline materials, instead of a metal silicide like a tungsten silicide(WSix).

Fig. 1 illustrates a layout of a semiconductor device having a COB(Capacitor Over Bitline) structure of prior art. Fig. 2a through Fig. 2d illustrate process sectional views for describing a fabricating method of a semiconductor device of prior art, illustrating sectional views in accordance with a 1A-1A' line of Fig. 1. Fig. 3a and Fig. 3d illustrate sectional views in accordance with a 1B-1B' line of Fig. 1 of a prior semiconductor device. Fig. 4 illustrates a sectional structure of a semiconductor device of prior art in

accordance with a 1C-1C' line of Fig. 1.

Referring to Fig. 2a and Fig. 3a, a semiconductor substrate(100) having active regions(101) and field regions is provided. Through a common STI(Shallow Trench Isolation) process, STI device separation films(105) are formed in the field regions of the semiconductor substrate(100).

Gates(110) are formed on the semiconductor substrate(100), having a deposited structure with a gate insulating film(111), a gate electrode material(113), and a capping layer(115), and forming a spacer(117) on a sidewall.

After forming a first interinsulation layer(120) on the entire surface of the substrate including the gates(110), a contact(125) exposing the active regions(101), for instance, an SAC(Self-Aligned Contact) is formed. And, contact pads(130) composed of a poly-silicon film and others are formed on the contact(125). At this time, though not shown in the diagram, the contact pads(130) are electrically connected to impurity regions having predetermined conductive types formed in the active regions(101).

Then, after depositing a second interinsulation layer(140) on the first interinsulation layer(120), corresponding contact pads of the contact pads(130), that is, bitline contacts(145) exposing the contact pads(130) to be connected with bitlines that will be formed in a next process are formed.

After depositing a metal film for the contact pads, for example, a

tungsten film on the entire surface of the substrate including the bitline contacts(145), the tungsten film is etched by a chemi-mechanical process(CMP) or an etch back process, thereby forming a contact pad(150) for the bitlines in the bitline contacts(145).

Referring to Fig. 2b and Fig. 3b, bitlines(160) having a deposited structure with a conductive material(161) for the bitlines and a capping layer(165) are formed by sequentially depositing the conductive material(161) for the bitlines like a tungsten film and the bitline capping layer(165) like a silicon film on a second interinsulation layer(140) and patterning them. The bitlines(160) are electrically connected to a contact pad(150) for the bitlines formed in bitline contacts(145). A bitline spacer(170) is formed by depositing a silicon film on the second interinsulation layer(140) including the bitlines(160) with an insulating film for the bitline spacer, and by etching the silicon film.

Referring to Fig. 2c and Fig. 3c, a third interinsulation layer(180) is formed on a second interinsulation layer(140) including the bitlines(160). By etching the second and the third interinsulation layers(140,180), a contact(185) for a storage node exposing corresponding contact pads of contact pads(130), that is, the contact pads(130) connected to the storage node formed in a next process is formed.

After depositing a poly-silicon film on the third interinsulation layer(180) to fill the contact(185) for the storage node, a contact pad(190) for the storage node is formed by separating the node with the use of a CMP method and

others. The contact pad(190) for the storage node is electrically connected to the contact pads(130) through the storage node contact(185). Then, a storage node(200) of a capacitor connected to the contact pad(190) for the storage node is formed.

A prior method forms bitlines by etching a metal film like a tungsten film through a photoetching process, thus there causes a problem of restrictions on an etching of a metal pattern having a small line/spacer due to high integration as well as causes process complexity.

In addition, since it is impossible to use cleaning solutions including OH radicals such as SC1(Standard Cleaning 1) with excellent detergency for particles and polymers while patterning a metal film for forming bitlines, it is unavailable to perfectly remove particles during cleaning process, causing defects owing to the particles.

To solve the above problems of prior art, a method of forming bitlines through a damascene process has been suggested. When forming bitlines of a semiconductor device having a COB structure with the use of a damascene process, it is necessary to surround the bitlines by forming materials having etching selectivity with an oxide film, an interinsulation layer, for instance, a capping layer and a spacer composed of silicon films on upper and side walls, in order to protect the bitlines during a next process of forming a storage node contact.

A technology of protecting the bitlines by perfectly surrounding a damascene bitline with the use of the capping layer and the spacer has been suggested in Korean Laid Open Publication No. 2001-55685. The above technology forms the bitlines perfectly surrounded by the spacer composed of the silicon film, thereby obtaining process margins by protecting the bitlines during the storage node contact process. However, it causes the increase of parasitic capacitance since the silicon film having a higher dielectric constant than that of an oxide film exists between neighboring bitlines.

[Technical Goal of the Invention]

It is therefore an object of the present invention to provide a semiconductor device and a fabrication method thereof for improving process margins while forming a storage node contact by forming a stud type bitline capping layer.

It is another object of the present invention to provide a semiconductor device and a fabricating method thereof for reducing parasitic capacitance between bitlines and between the bitlines and a storage node contact by surrounding the bitlines with an oxide film.

[Structure and Operation of the Invention]

To solve the above objects, the present invention provides a semiconductor device, comprises: an insulating film formed on a semiconductor substrate, and having bitline contacts and groove-type bitline patterns; bitlines formed in a portion of the bitline contacts and the bitline

patterns, and surrounded by the insulating film; and a bitline capping layer formed on the bitlines within the bitline patterns and the insulating film, to be protruded than the insulating film, and wherein a protruded part is wider than width of the bitlines.

The bitline capping layer comprises: a first capping material with a pillar type protruded than the insulating film on the bitlines within the bitline patterns; and a second capping material formed as a sidewall spacer type in a protruded part of the first capping material of the insulating film. It is desirable that the protruded part of the first capping material should be protruded in a half thickness of the first capping material.

In addition, the present invention provides a method of fabricating a semiconductor device, comprising the steps of: forming an insulating film on a semiconductor substrate; etching the insulating film, and forming bitline contacts and groove-type bitline patterns; forming bitlines formed in a portion of the bitline contacts and the bitline patterns; and forming a bitline capping layer protruded than the insulating film and wider than width of the bitlines on the bitlines of the bitline patterns and the insulating film.

Furthermore, the present invention provides a semiconductor device, comprising: a first insulating film formed on a semiconductor substrate, and having many contacts exposing the semiconductor substrate; contact pads for bitlines and contact pads for a storage node formed on each contact; a second insulating film formed in the first insulating film, and having bitline contacts exposing the contact pads for the bitlines and groove-type bitline patterns;

bitlines formed in a portion of the bitline contacts and the bitline patterns, and surrounded by the second insulating film; a bitline capping layer formed in the bitline patterns and the second insulating film, to be protruded than the second insulating film, and wherein the protruded part is wider than width of the bitline patterns; a third interinsulation layer formed on the entire surface of the substrate; and a storage node contact formed in the second and the third insulating films to expose the contact pads for the storage node.

In addition, the present invention provides a method of fabricating a semiconductor device, comprising the steps of: forming a first insulating film having contact pads for bitlines and contact pads for a storage node on a semiconductor substrate; forming a second insulating film on the entire surface of the substrate; forming bitline contacts for exposing the contact pads for the bitlines by etching the second insulating film, and forming groove-type bitline patterns; forming bitlines in a portion of the bitline patterns, to be connected with the contact pads for the bitlines through the bitline contacts; forming a bitline capping layer protruded than the second insulating layer, and wherein a protruded part is wider than width of the bitline patterns, in the bitlines within the bitline patterns and the insulating film; forming a third insulating film on the entire surface of the substrate; and forming a storage node contact by etching the second and the third insulating films, to expose the contact pads for the storage node.

Moreover, the present invention provides a method of fabricating a semiconductor device, comprising the steps of: forming a first insulating film

having contact pads for bitlines and contact pads for a storage node on a semiconductor substrate; sequentially forming a second insulating film, an etching interception film, and a third insulating film on the entire surface of the substrate; forming bitline contacts for exposing the contact pads for the bitlines by etching the second/the third insulating films and the etching interception film, and forming groove-type bitline patterns; forming bitlines in a portion of the bitline patterns, to be connected with the contact pads for the bitlines through the bitline contacts; filling the bitlines of the bitline patterns with a first capping material; etching the third insulating film by using the etching interception film, to expose the first capping material; depositing a second capping material on the entire surface of the substrate; etching the second capping material and the etching interception film, and leaving the etched ones in a protruded part only of the first capping material; forming a fourth insulating film on the entire surface of the substrate; forming a storage node contact for exposing the contact pads for the storage node by etching the third and the fourth insulating films. The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate or intervention layers may be also be present.

Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

Hereinafter, the prior art will be described with reference to the accompanying drawings.

Figs. 5a through 5i are process sectional views illustrating a fabricating method of a semiconductor device having a COB structure in accordance with one embodiment of the present invention, illustrating the sectional vies corresponding to a 1A-1A' line of Fig. 1. Figs. 6a through 6i illustrate process sectional views for describing a fabricating method of a semiconductor device in accordance with one embodiment of the present invention, illustrating the sectional views corresponding to a 1B-1B' line of Fig. 1. Figs. 7a through 7i illustrate process sectional views for describing a fabricating method of a semiconductor device in accordance with one embodiment of the present invention, illustrating the sectional views corresponding to a 1C-1C' line of Fig. 1.

Referring to Fig. 5a, Fig. 6a, and Fig. 7a, a semiconductor substrate(300) having active regions(301) and field regions is provided. An STI device separation film(305) is formed in the field regions of the semiconductor substrate(300) through a common STI(Shallow Trench Isolation) process.

After depositing a first interinsulation layer(320) on the entire surface of the substrate including gates(310), a contact(325) exposing the active regions(301), for instance, an SAC(Self-Aligned Contact) is formed. And,

contact pads(330) composed of conductive materials like poly-silicon films are formed on the contact(325). At this time, though not shown in the diagram, the contact pads(330) are electrically connected to impurity regions having predetermined conductive types formed in the active regions(301).

Then, after depositing a second interinsulation layer(340) on the first interinsulation layer(320), smooth the deposited layer by performing a CMP or an etch back process. At this time, the second interinsulation layer(340) deposits insulating films with oxide film series such as HDP(High Density Plasma) oxide film, BPSG film and others in 4500 to 5000Å thickness.

Referring to Figs. 5b, 6b, and 7b, bitline contacts(345) and bitline patterns(355) are formed by etching a second interinsulation layer(340) through a dual damascene process. At this time, the bitline contacts(345) are formed to expose corresponding contact pads of contact pads(330), that is, contact pads connected to bitlines that will be formed in a next process. The bitline patterns(355) are formed to cross with gates(310), having groove types.

When forming the bitline contacts(345) and the bitline patterns(355) by etching the second insulation layer(340) through the dual damascene process, it is possible to form the bitline patterns(355) after forming the bitline contacts(345) or form the bitline contacts(345) after forming the bitline patterns(355). At this point, the bitline contacts(345) are formed by etching the second insulation layer(340), making the contact pads(330) etching

interception films.

Referring to Figs. 5c, 6c, and 7c, a conductive material(361) for bitlines, for instance, a tungsten film is deposited on a second insulation layer(340) including bitline contacts(345) and bitline patterns(355). Referring to Fig. 5d, 6d, and 7d, by over-etching a conductive material(361) for bitlines, the over-etched conductive material is left in a portion of bitline patterns(355) including bitline contacts(345).

On this occasion, it is desirable that the bitline patterns(355) have 2500 Å in depth and a conductive material(362) for bitlines remaining in the bitline patterns(355) has 500Å in depth. The conductive material(361) for the bitlines can be etched by using a CMP or an etch back(360) process, or etched by using all the CMP and the etch back process.

In an embodiment of the present invention, the bitline contacts(345) are also filled when the bitline patterns(355) are filled with the conductive material for the bitlines, rather than filling the bitline patterns(355) with the conductive material for the bitlines after forming a contact plug in the bitline contacts(345) through another process.

Referring to Figs. 5e, 6e, and 7e, a bitline conductive material(362) of bitline patterns(355) is filled with a first capping material(365) by a CMP or an etch back process after depositing the first capping material(365) for bitlines

on a second interinsulation layer(340) including the bitline patterns(355).

Referring to Figs. 5f, 6f, and 7f, after dry-etching or wet-etching a second interinsulation layer(340) to protrude a silicon film(365) in certain thickness, a second capping material(366) for bitlines is deposited on the entire surface of a substrate. At this moment, it is desirable to etch the second interinsulation layer(340) in a half thickness of the silicon film(365) formed on a bitline conductive material(362).

Therefore, supposing that the bitline patterns(355) has 2500Å in depth and the conductive material(362) for bitlines has 500Å in thickness, it is desirable to etch the second interinsulation layer(340) in thickness of 1000Å. The first capping material(365) and the second capping material(366) have wet and dry etching selectivity with the second interinsulation layer(340) with an oxide film series, using silicon films and others.

Referring to Figs. 5g, 6g, and 7g, by etching back the silicon film(365), a sidewall only of a protruded part of the silicon film(365) is made in a type of a spacer(367).

Thus, capping layers(369) for bitlines are formed, composed of the first capping material(365) with a pillar type formed on a conductive material(362) for bitlines and the second capping material(367) with the spacer type formed on the sidewall of the first capping material(365).

At this time, a part surrounded by a second insulation layer(340) of the capping layers(369) for the bitlines has the same width as bitline patterns, and the protruded part becomes bigger than width of the bitline patterns(355). Therefore, bitlines(360) are formed, having the conductive material(362) formed in the bitline patterns(355) and the stud type capping layers(369) formed in the conductive material(362) and the second interinsulation layer(340).

Among the capping layers(369), the second capping material(367) with the spacer type is formed to surround a sidewall portion only of the first capping material(365) with the pillar type, thus the conductive material(362) for the bitlines is surrounded by the second interinsulation layer(340) with an oxide film series.

On this occasion, the second capping material(365) is surrounded in a half thickness only of the first capping material(362), because it can obtain process margins while forming a storage node contact in a next process as well as maintain insulating properties, and reduce parasitic capacitance between the bitlines(360) and the bitlines(360) and between the bitlines(360) and storage node contacts formed in a next process.

Referring to Figs. 5h, 6h, and 7h, corresponding contact pads of contact pads(330), that is, a storage node contact(375) exposing contact pads connected with a storage node that will be formed in a next process is formed

by depositing a third interinsulation layer(370) with an oxide film series on the entire surface of a substrate and etching a second and the third interinsulation layers(340, 370). The second and the third interinsulation layers(340, 370) are self align-etched because a spacer(367) of bitline capping layers(369) operates as an etching interception layer, thereby forming a storage node contact(375) to a self align contact.

Referring to Figs. 5i, 6i, and 7i, after depositing a conductive material like a poly-silicon film on a third interinsulation layer(370) including the storage node contact(375), smooth the deposited conductive material through a CMP or an etch back process, thereby forming a contact plug(380) for a storage node. And, a storage node(390) of a capacitor electrically connected with the contact plug(380) for the storage node is formed.

Like shown above, with a method of fabricating a semiconductor device in accordance with one embodiment of the present invention, the storage node contact(375) is self align-etched and obtains sufficient etching process margins since capping layers operate as etching interception layers, during an etching process of forming the storage node contact, by forming bitline capping layers in stud types. In addition, since the second and the third interinsulation layers(340, 370) with oxide film series having lower dielectric constants than those of silicon films exist between the bitlines(360) and between the bitlines(360) and the contact plug(380) for the storage node, it can reduce parasitic capacitance between them.

Fig. 11a is a diagram illustrating relations between thickness of a bitline

capping layer and parasitic capacitance. It is found that a reduced threshold value of the parasitic capacitance in accordance with the thickness of the bitline capping layer composed of a silicon film is 1000Å. Fig. 11b is a diagram illustrating relations between a bitline spacer and parasitic capacitance. 'A' shows distribution of the parasitic capacitance in a case when all bitline spacers are composed of oxide films, and 'C' shows a case when all the bitline spacers are composed of silicon films, then 'B' shows distribution of the parasitic capacitance in a case when partial bitline spacers are composed of oxide films, that is, when oxide films exist between bitlines and silicon films exist between the bitlines and a storage node contact. Referring to Fig. 11b, it is found that the parasitic capacitance has been reduced by 30% and 40%, respectively, in the case when the bitline spacers are fully composed of oxide films(A) or partially composed of silicon films and oxide films(B), rather than the case when all the bitline spacers are composed of silicon films(C).

Seeing Figs. 11a and Fig. 11b, the present invention can minimize the parasitic capacitance as maintaining insulating properties by forming stud type bitline capping layers, and also improve process margins for forming a storage node contact.

Fig. 8a through Fig. 8d, Fig. 9a through Fig. 9d, and Fig. 10a through Fig. 10d illustrate process sectional views in accordance with another embodiment of the present invention. Fig. 8a through Fig. 8d are process sectional views corresponding to a 1A-1A' line of Fig. 1. Fig. 9a through Fig. 9d are process sectional views corresponding to a 1B-1B' line of Fig. 1. Fig. 10a

through Fig. 10d are process sectional views corresponding to a 1C-1C' line of Fig. 1.

A method of fabricating a semiconductor device in accordance with another embodiment of the present invention is the same as the process of the first embodiment, however, it is different in terms of forming a second interinsulation layer with a deposited structure where a silicon film for etching interception is sandwiched between an upper oxide film and a lower oxide film, in order to obtain etching stability in an etching process of forming a capping spacer.

Referring to Figs. 8a, 9a, and 10a, a semiconductor substrate(500) having active regions(501) and field regions is provided. An STI device separation film(505) is formed in the field regions of the semiconductor substrate(500) through a common STI(Shallow Trench Isolation) process.

Gates(510) having a deposited structure with a gate insulating film(511), a gate electrode material(513), and a capping layer(515) are formed on the semiconductor substrate(500), and a gate spacer(517) is formed on a sidewall of the gates(510).

After depositing a first interinsulation layer(520) on the entire surface of the substrate including the gates(510), a contact(525) exposing the active regions(501) between the gates(510) is formed, and contact pads(530) composed of a poly-silicon film is formed in the contact(525). At this moment,

though not shown in the diagram, the contact pads(530) are connected to impurity regions having predetermined conductive types formed in the active regions(501) through the contact(525).

Then, second interinsulation layers(550) are deposited on the first interinsulation layer(520), and formed with a deposited structure of a lower oxide film(551), a silicon film(552), and an upper oxide film(553). The upper oxide film(553) is removed while forming a capping spacer in a next process, and the silicon film(552) operates as an etching interception film when etching the upper oxide film(553).

Referring to Figs. 8b, 9b, and 10b, a bitline contact(545) and a bitline pattern(555) are formed through a dual damascene process. At this moment, when etching second interinsulation layers(550), it should be etched without any etching selectivity between upper, lower oxide films(551, 553) and a silicon film(552).

While forming the bitline contact(545) and the bitline pattern(555) through the dual damascene process, it is possible to form the bitline pattern(555) after forming the bitline contact(545), or to form the bitline contact(545) after forming the bitline pattern(555). On this occasion, when forming the bitline contact(545), contact pads(530) operate as etching interception films.

Then, after depositing a conductive material for bitlines, for instance, a

tungsten film on the second interinsulation layers(550) including the bitline contact(545) and the bitline pattern(555), a portion of the bitline pattern(555) should be filled with a conductive material(562) for bitlines by an over CMP or an etch back process. At this point, the conductive material(562) for the bitlines should be filled in a lower part than the silicon film(552) within the bitline pattern(555). That is, thickness of the conductive material(562) for the bitlines should be thinner than that of the lower oxide film(551).

Next, after depositing a first capping material for bitlines, for example, a silicon film on the second interinsulation layers(550) including the bitline pattern(555), the conductive material(562) for the bitlines of the bitline pattern(555) is filled with a silicon film(565) by a CMP or an etch back process.

Referring to Figs. 8c, 9c, and 10c, an upper oxide film(553) of the second interinsulation layer(550) is dry or wet etched. It is possible to stably remove the upper oxide film(553) by using a silicon film(552) as an etching interception film.

Referring to Figs. 8d, 9d, and 10d, after depositing a material having dry/wet etching differences with a lower oxide film(551), for instance, a silicon film on the entire surface of a substrate as a second capping material for bitlines, a spacer(567) is formed on a sidewall of the silicon film(565) by etching the deposited silicon film. At this time, when etching the silicon film, the second capping material for the bitlines, the silicon film(552) is also etched, thereby exposing the lower oxide film(551).

Therefore, capping layers(569) for bitlines are formed, composed of the first capping material(565) with a pillar type formed on the conductive material(562) for bitlines and the second capping material(567) with a spacer type formed on the sidewall of the first capping material(565). So, bitlines(560) are formed, having a conductive material(562) formed within the bitline pattern(555) and the stud type capping layers(569) formed on the conductive material(562) and second interinsulation layer(540).

At this time, the second capping material(567) with the spacer type is surrounded in a half thickness of a sidewall portion of the first capping material(565) with the pillar type, for instance, the first mapping material(565), since it can reduce parasitic capacitance as well as obtain insulating properties and process margins.

Though not shown in the diagram, after depositing a third interinsulation layer, a storage node contact is formed by etching the third interinsulation layer and the lower oxide film(551), and a contact plug for a storage node is formed in the storage node contact, then a storage node of a capacitor electrically connected with the contact plug is formed.

In the embodiment of the present invention, though the bitlines are formed by depositing the conductive material for the bitlines only, it is possible to form the bitlines by depositing the conductive material for the bitlines after depositing a barrier metal film like TiN.

[Effect of the invention]

According to the present invention like above, it can obtain sufficient process margins while forming a storage node contact by forming capping layers of bitlines with study types, as well as reduce contact resistance by increasing contact open regions. In addition, it can decrease parasitic capacitance, since an oxide film whose dielectric constant is lower than that of a silicon film exists between the bitlines and between the bitlines and the storage node contact.

It is to be understood that changes and modifications to the embodiments described above will be apparent to those skilled in the art, and are contemplated. It is therefore intended that the foregoing detailed description be regarded as illustrative rather than limiting, and that it be understood that it is the following claims, including all equivalents, that are intended to define the spirit and scope of this invention.

WHAT IS CLAIMED IS

1. A semiconductor device, comprises:

an insulating film formed on a semiconductor substrate, and having bitline contacts and groove-type bitline patterns;

bitlines formed in a portion of the bitline contacts and the bitline patterns, and surrounded by the insulating film; and

a bitline capping layer formed in the bitlines of the bitline patterns and the insulating film, to be protruded than the insulating film, and wherein a protruded part is wider than width of the bitlines.

2. The semiconductor device of claim 1, wherein the bitline capping layer, comprises:
a first capping material with a pillar type protruded than the insulating film in the bitlines of the bitline patterns; and
a second capping material formed in a sidewall spacer type in the protruded part of the first capping material on the insulating film.

3. The semiconductor device of claim 2, wherein the protruded part of the first capping material of the bitline capping layer is protruded in a half thickness of the first capping material.

4. The semiconductor device of claim 1, wherein the bitline capping layer is composed of a material having wet and dry etching differences with the insulating film.

5. The semiconductor device of claim 4, wherein the bitline capping layer is composed of a film with a silicon film series, and the insulating film is composed of a film with an oxide film series.

6. The semiconductor device of claim 1, wherein the bitline capping layer has a stud type structure.

7. A method of fabricating a semiconductor device, comprising the steps of:

forming an insulating film on a semiconductor substrate;

etching the insulating film, and forming bitline contacts and groove-type bitline patterns;

forming bitlines formed in a portion of the bitline contacts and the bitline patterns; and

forming a bitline capping layer protruded than the insulating film and whose protruded part is wider than width of the bitlines in the bitlines of the bitline patterns and the insulating film.

8. The method of claim 7, wherein the method of forming the bitline capping layer, comprises the steps of:

depositing a first capping material on the entire surface of the substrate;

etching the first capping material, and filling the bitline patterns located in an upper part of the bitlines with the etched material;

etching the insulating film in a certain thickness, to protrude a portion of the first capping material;

depositing a second capping material having etching differences with the insulating film on the entire surface of the substrate; and

etching the second capping material, and leaving the etched second capping material on a sidewall only of the protruded part of the first capping material.

9. The method of claim 8, wherein the first capping material of the bitline capping layer is etched to be protruded in a half thickness of the first capping

material.

10. The method of claim 8, wherein the first and the second capping materials are composed of materials having wet and dry etching differences with the insulating film.

11. The method of claim 10, wherein the first and the second capping materials are composed of films with silicon film series, and the insulating film is composed of a film with an oxide film series.

12. The method of claim 8, wherein the insulating film is etched through a wet or a dry etching process.

13. The method of claim 7, wherein the bitline capping layer, comprises:
a first capping material with a pillar type protruded than the insulating film of the bitlines within the bitline patterns; and a second capping material formed in a sidewall spacer type in a protruded part of the first capping material on the insulating film, having a stud type structure.

14. The method of claim 7, wherein the method of forming the bitlines within the bitline patterns, comprising the steps of:
depositing a conductive material for the bitlines on the entire surface of the substrate to fill the bitline patterns; and
etching the conductive material for the bitlines, and forming the bitlines filled up to a certain depth of the bitline patterns.

15. The method of claim 14, wherein the bitlines over-etch the conductive material for the bitlines by using a CMP, an etch back process or the CMP and the etch back process.

16. The method of claim 7, wherein the bitline patterns are formed after forming the bitline contacts by using the dual damascene process.

17. The method of claim 7, wherein the bitline contacts are formed after forming the bitline patterns by using the dual damascene process.

18. A semiconductor device, comprises:

a first insulating film formed on a semiconductor substrate, and having many contacts exposing the semiconductor substrate;

contact pads for bitlines and contact pads for a storage node formed in each contact;

a second insulating film formed in the first insulating film, and having bitline contacts exposing the contact pads for the bitlines and groove-type bitline patterns;

bitlines formed in a portion of the bitline contacts and the bitline patterns, and surrounded by the second insulating film;

a bitline capping layer formed in the bitline patterns and the second insulating film, to be protruded than the second insulating film, and whose protruded part is wider than width of the bitline patterns;

a third interinsulation layer formed on the entire surface of the substrate; and

a storage node contact formed in the second and the third insulating films, to expose the contact pads for the storage node.

19. A method of fabricating a semiconductor device, comprising the steps of:
forming a first insulating film having contact pads for bitlines and contact pads for a storage node on a semiconductor substrate;
forming a second insulating film on the entire surface of the substrate;
etching the second insulating film, and forming bitline contacts exposing the contact pads for the bitlines and groove-type bitline patterns;
forming bitlines in a portion of the bitline patterns, to be connected with the contact pads for the bitlines through the bitline contacts;
forming a bitline capping layer protruded than the second insulating film, and whose protruded part is wider than width of the bitline patterns in the bitlines of the bitline patterns and the insulating film;
forming a third insulating film on the entire surface of the substrate; and
etching the second and the third insulating films to expose the contact pads for the storage node, and forming a storage node contact.

20. The method of claim 19, wherein after forming the bitline contacts by making the contact pads for the bitlines etching interception films with the use of a dual damascene process and etching the second insulating film, and the bitline patterns are formed by etching the second insulating film.

21. The method of claim 19, wherein after forming the bitline patterns by etching the second insulating film with the use of the dual damascene process,

the bitline contacts are formed by making the contact pads for the bitlines etching interception films and etching the second insulating film.

22. The method of claim 19, wherein the bitline capping layer, comprises:
a first capping material with a pillar type protruded than the second insulating film in the bitlines of the bitline patterns; and a second capping material formed in a sidewall spacer type in a protruded part of the first capping material on the second insulating film, having a stud type structure.

23. The method of claim 22, wherein the storage node contact is self align-etched when the second and the third insulating films form the second capping material of the bitline capping layer as an etching interception film.

24. The method of claim 22, wherein the first capping material of the bitline capping layer is protruded in a half thickness of the first capping material.

25. A method of fabricating a semiconductor device, comprising the steps of:
forming a first insulating film having contact pads for bitlines and contact pads for a storage node on a semiconductor substrate;
sequentially forming a second insulating film, an etching interception film, and a third insulating film on the entire surface of the substrate;
etching the second and the third insulating films and the etching interception film, and forming bitline contacts exposing the contact pads for the bitlines and groove-type bitline patterns;
forming bitlines in a portion of the bitline patterns, to be connected with the

contact pads for the bitlines through the bitline contacts;

filling the bitlines of the bitline patterns with a first capping material;

etching a third insulating film by using the etching interception film, to protrude the first capping material;

depositing a second capping material on the entire surface of the substrate;

etching the second capping material and the etching interception film, and leaving the etched material and the film on a sidewall only of the protruded part of the first capping material;

forming a fourth insulating film on the entire surface of the substrate; and

etching the third and the fourth insulating films, and forming a storage node contact exposing the contact pads for the storage node.

26. The method of claim 25, wherein the second and the third insulating films have oxide film series, and the etching interception film is a material having etching differences with the second and the third insulating films and is composed of a silicon film series.

27. The method of claim 25, wherein the second to the fourth insulating films have oxide film series, and the first and the second bitline capping materials have etching differences with the second to the fourth insulating films and composed of films with silicon film series.

28. The method of claim 25, wherein the protruded part of the first capping material has a half thickness of the first capping material.

29. The method of claim 25, wherein the bitline node contact is formed by self align-etching the second to the fourth insulating films after making the bitline capping layer an etching interception film.